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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
CAMPOS, YAIMA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,342	ANAND, ANUPAM	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 24-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 24-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. As per the instant Application having Application number 10/726,342, the examiner acknowledges the applicant's submission of the amendment dated June 28, 2007. At this point, claims 1, 3-4, 6, 8-15 and 24-27 have been amended and claims 16-23 and 28-40 stand cancelled. There are 19 claims pending in the application; there are 4 independent claims and 15 dependent claims, all of which are ready for examination by the examiner. Claims 1-15 and 24-27 are pending.

AMENDMENT TO DRAWINGS AND SPECIFICATION

2. The amendments to the Drawings and Specification filed on June 28, 2007 are deemed proper and have been entered.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim 24** is rejected under 35 U.S.C. 102(b) as being anticipated by Goldberg (US 6,874,062).

5. As per **claim 24**, Goldberg discloses a method for managing memory, the method comprising: analyzing a state of a first logic circuit to determine whether a block of memory

segments includes a memory segment that is available for data storage, the first logic circuit having a first state when the block of memory segments has a memory segment that is available for data storage and a second state when the block of memory segments does not have a memory segment that is available for data storage; and if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage **[Goldberg discloses this limitation as "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) and explains performing "a search for an available storage Segment of a predetermined length" (Col. 11, lines 23-28) (Figures 8A-9D and related text)].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-15 and 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg (US 6,874,062) in view of Lehman (US 6,658,437).

8. As per **claims 1 and 25**, Goldberg discloses

A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: **[Goldberg discloses "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "Files can further be subdivided into smaller addressable portions of memory called "sections," wherein each section has a same predetermined size" (Col. 7, lines 22-26) and explains grouping sections into segments (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]**

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage **["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one**

correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)].

wherein the first state includes at least a portion of a memory address of the first memory block

[Goldberg discloses "in step 814 processing is completed and the memory address associated with the located available memory sections may be returned to the requested" (Col. 12, line 26-29) and discloses "a data structure that may be used to store the Hierarchical Bitmap Structure of the current invention... a level descriptor for each of the individual bitmaps in the Bitmap Packet 1002. This level descriptor includes information such as the starting address and bit-length of the corresponding bitmap" (Col. 15, lines 19-40; Figure 10 and related text)].

Goldberd does not explicitly disclose the details of having the first state include at least a portion of a memory address of the first memory block.

Lehman discloses having the first state includes at least a portion of a memory address of the first memory block as **["The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30... the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability" (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein "blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array... For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks" (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text); therefore, having bits which represent a first state which indicates availability of a memory block comprise *at least a portion* of a memory address of a memory block as the bit position indicating available memory indicates the address/position/location of the available memory block]**.

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further

the first state includes at least a portion of a memory address of the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses **["a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)]**.

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claims 1 and 25.

9. As per **claim 2**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second state when the first memory segment is not available for data storage **[Goldberg discloses "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text)]**.

10. As per **claim 3**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 1, wherein the second state is a state of a single logic bit **[Goldberg discloses "a bit is set if a Section is in use and is cleared if the Section is available for**

allocation" (Col. 7, lines 50-61). Lehman also discloses this limitation, as a bit is 1 to represent allocated memory (See Figure 9 and related text) which corresponds to a second state].

11. As per **claim 4**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 1 wherein the second state comprises information of an offset to a next available memory block or memory segment **[Goldberg discloses "by skipping portions of the LLB that are not associated with available memory, the search is completed more efficiently" (Col. 10, lines 25-29). Lehman discloses "pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size" (Col. 9, lines 53-60) wherein "the pointer array 124 might point to a buddy segment that is available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment" (Col. 10, lines 1-10) (Figure 7 and related text); therefore, a memory state indicating certain portions of memory are not available comprises information of the location of free/available memory].**

12. As per **claim 5**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory

segment is not available for data storage **[Goldberg discloses "in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

13. As per **claim 6**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 2, wherein the first state of the second logic circuit comprises at least a portion of a memory address of the first memory segment **[Lehman discloses "The DBMS 24 receives database requests from the clients 28 and performs data access operations to storage and retrieve referenced data values from the storage subsystem 30... the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability" (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein "blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array... For example, for size=1, the pattern 1100 1111 0011**

0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks" (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text); therefore, having bits which represent a first state which indicates availability of a memory block comprise *at least a portion* of a memory address of a memory block as the bit position indicating available memory indicates the address/position/location of the available memory block].

14. As per **claim 7**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 2, and explains **[Goldberg discloses this limitation as in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text) and explains performing a top-down search of hierarchical bitmap structures in which "if such a string is located, processing continues... If an address is returned indicating that the desired available memory had been located, each of the bits in the Current_BML that corresponds to a bit described by Saved_Bits must be set to an appropriate state... the state indicated whether or not the bit corresponds to memory that has been entirely allocated" (Col. 14, lines 38-57) (Figures 8A-9D and related text)]** Lehman discloses a third logic circuit that converts the first state of the first logic circuit and the first state

of the second logic circuit to the memory address of the first memory segment as **["blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array" (Col. 10, line 61-Col. 11, line 5) (Figure 9 and related text)]**.

15. As per **claim 8**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 2, wherein the first and second states of the first logic circuit are states of a plurality of logic bits and the first and second states of the second logic circuit are states of a plurality of digital bits **[Lehman discloses "the second type of allocation bit map, where size=0, is used for blocks that are sixteen times the unit size, or larger... In the second type bit map, the first byte is the status byte for the buddy segment" (Col. 11, lines 47-57); therefore, having a plurality of bits representing states/status]**.

16. As per **claim 9**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 2, wherein the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment **[Goldberg discloses this limitation as in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond**

to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text) and explains performing a top-down search of hierarchical bitmap structures in which "if such a string is located, processing continues... If an address is returned indicating that the desired available memory had been located, each of the bits in the Current_BML that corresponds to a bit described by Saved_Bits must be set to an appropriate state... the state indicated whether or not the bit corresponds to memory that has been entirely allocated" (Col. 14, lines 38-57) (Figures 8A-9D and related text)].

17. As per **claims 10 and 26**, Goldberg discloses a memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising: **[Goldberg discloses "an Operating System (OS) 200 running on IP 104 manages and allocates the various resources of Data Processing System" (Col. 7, lines 11-13) wherein "Files can further be subdivided into smaller addressable portions of memory called "sections," wherein each section has a same predetermined size" (Col. 7, lines 22-26) and explains grouping sections into segments (Col. 8, lines 49-65) (Figures 1 and 2 and related text)]**

a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; **["in a hierarchical bitmap scheme... the Lowest**

Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)] wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block **[With respect to this limitation, Goldberg discloses "a bitmap structure is defined that allows N contiguous search items to be located wherein all search items in the set have a same predetermined attribute. The system and method may be adapted for use in locating N contiguous sections of memory all having the same predetermined attribute. Namely the contiguous sections are all available for allocation" (Col. 8, line 23-32)]** but does not expressly disclose the details of wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block.

Lehman discloses wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block as **["for the first type of bit map, where the size bit is set to size=1, the bits are examined as individual bits, and logical groups inside the 16 bits must be determined by examining adjacent bits. For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided" (Col. 11, lines 6-14)]**.

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further the first state comprise information indicating a number of available memory segments in the first memory block as taught by Lehman.

The motivation for doing so would have been because Lehman discloses **["a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)]**.

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claims 10 and 26.

18. As per **claim 11**, the combination of Goldberg and Lehman discloses the memory management circuit of claim 10, further comprising: a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage; **["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB) in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) wherein "each of the bits in Bitmap 316 correspond to an associated one of Sections 0 trough 7... a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61) (Figure 3 and related text). Goldberg further discloses "additional hierarchical levels within the bitmap may be created... bitmap 1 may be subdivided into Segments" (Col. 10, lines 34-37) (Figures 5-6 and related text)]**.

19. As per **claim 12**, the combination of Goldberg and Lehman discloses The memory management circuit of claim 11, wherein the first and second states of the second logic circuit are single-bit logic states **[The rationale in the rejection of claim 3 is herein incorporated]**.

20. As per **claims 13-15 and 27**, Goldberg discloses a memory management system for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising: a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; **["in a hierarchical bitmap scheme... the Lowest Level Bitmap (LLB)**

in the hierarchy is the bitmap which has a one-to-one correspondence with Memory Sections. That is, the LLB contains a bit for each Section in a File" (Col. 8, lines 43-48) and explains "the LLB may be divided into Segments... these Segments all include a same predetermined number of bits... a bitmap is then created to define the Segments of the LLB. This bitmap, which may be referred to as Bitmap 1, will include a corresponding bit to describe an associated different one of the Segments of the LLB... indicating the availability of memory... a bit in Bitmap 1, is set to "0" if any of the bits in the corresponding LLB are also cleared. A bit in Bitmap 1 will be in the second state if all bits in the corresponding LLB Segment are in a state indicating the unavailability of memory... a bit in Bitmap 1 is set to "1" if all bits in the corresponding LLB Segment are set" (Col. 8, lines 49-65) (Figures 5-6 and related text) wherein "a bit is set if a Section is in use and is cleared if the Section is available for allocation" (Col. 7, lines 50-61)].

wherein the second state of the first logic circuit comprise information indicating an offset to available memory **[Goldberg discloses "by skipping portions of the LLB that are not associated with available memory, the search is completed more efficiently" (Col. 10, lines 25-29)]** but doesn't expressly disclose the second state of the first logic circuit comprise information indicating an offset to available memory.

Lehman discloses the second state of the first logic circuit comprise information indicating an offset to available memory as **["pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size" (Col. 9, lines 53-60) wherein "the pointer array 124 might point to a buddy segment that is**

available, but on other occasions the pointer array might point to a segment that was recently allocated. Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment" (Col. 10, lines 1-10) (Figure 7 and related text); therefore, a memory state indicating certain portions of memory are not available comprises information of the location of free/available memory].

Goldberg (US 6,874,062) and Lehman (US 6,658,437) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory management circuit of claim 1 as taught by Goldberg and further specifically have the second state of the first logic circuit comprise information indicating an offset to available memory as taught by Lehman.

The motivation for doing so would have been because Lehman discloses **["a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)]**.

Therefore, it would have been obvious to combine Lehman (US 6,658,437) with Goldberg (US 6,874,062) for the benefit of creating a memory management circuit to obtain the invention as specified in claims 13-15 and 27.

ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

21. Applicant's arguments filed on June 28, 2007 have been considered but are not persuasive.

22. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

23. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

FIRST POINT OF ARGUMENT

24. Regarding Applicant's remark that the combination of Goldberg and Lehman does not disclose "a first logic circuit associated with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage, wherein the first state comprises at least a portion of a memory address of the first memory block" as Lehman discloses determining the address of a block based on bit position in the base group but does not disclose that "a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;" the Examiner respectfully disagrees.

Applicant should note that Lehman discloses "a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;" as **["The DBMS 24 receives database requests from the clients 28 and**

performs data access operations to storage and retrieve referenced data values from the storage subsystem 30... the DBMS 24 maintains data structures called allocation pages that keep track of data storage availability" (Col. 3, line 61-Col. 4, line 37) having an allocation array wherein "blocks larger than 1 can start only on an appropriate block address... the bit string 1111 1100 0000 0011, represents one allocated block of size 4, one allocated block of size 2, one free block of size 2, one free block of size 4, one free block of size 2, and one allocated block of size two" (Col. 11, lines 38-46) (Figure 7 and related text) and explains "the address of a block is determined by the bit position in the base group and by the position of the base group in the larger allocation array... For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks" (Col. 10, line 50-Col. 11, line 15) (Figure 9 and related text). ***The address 8 has a state of 0, indicating there is a memory unit available and having*** *"a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;"*]. Therefore, having bits which represent a first state which indicates availability of a memory block comprise *at least a portion* of a memory address of a memory block as the bit position having a state indicating available memory indicates the address/position/location of the available memory block. Furthermore, Applicant should note that Lehman discloses "a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;" because Applicant's specification clearly describes determining address portions of

memory segments based on the position of the identified block flag (Description of Figure 3) which is clearly disclosed by Lehman (See above).

25. Applicant's arguments stating that Applicant could not find portions of the amended claimed limitations have been considered and the Examiner has identified portions in the cited prior art that meet these limitations (See claim rejections above).

26. All arguments by the applicant are believed to be covered in the body of the office action; thus, this action constitutes a complete response to the issues raised in the remarks dated June 28, 2007.

CLOSING COMMENTS

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's Note

27. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

28. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

29. Per the instant office action, claims 1-15 and 24-27 have received a second action on the merits and are subject of a final rejection.

b. DIRECTION OF FUTURE CORRESPONDENCES

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

31. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 10, 2007

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100